

FIG. 1(PRIOR ART)

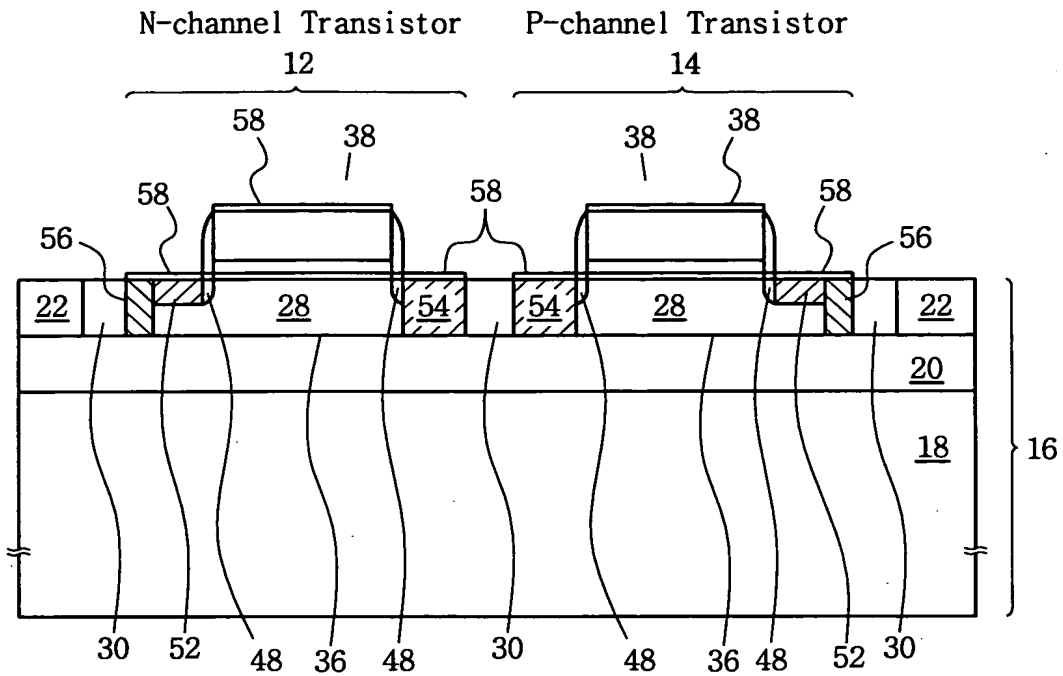


FIG. 2(PRIOR ART)

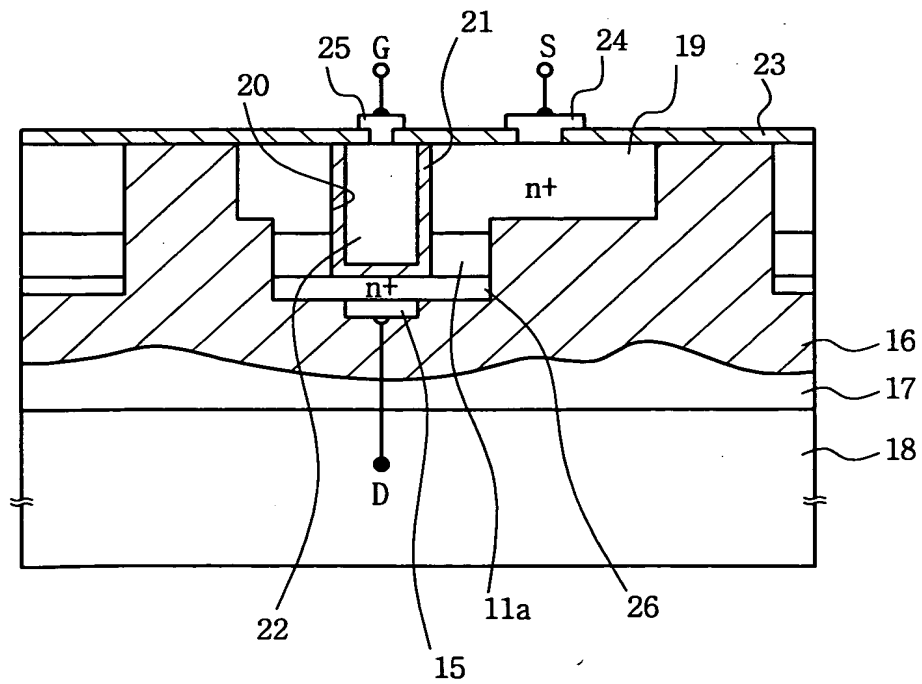


FIG. 3

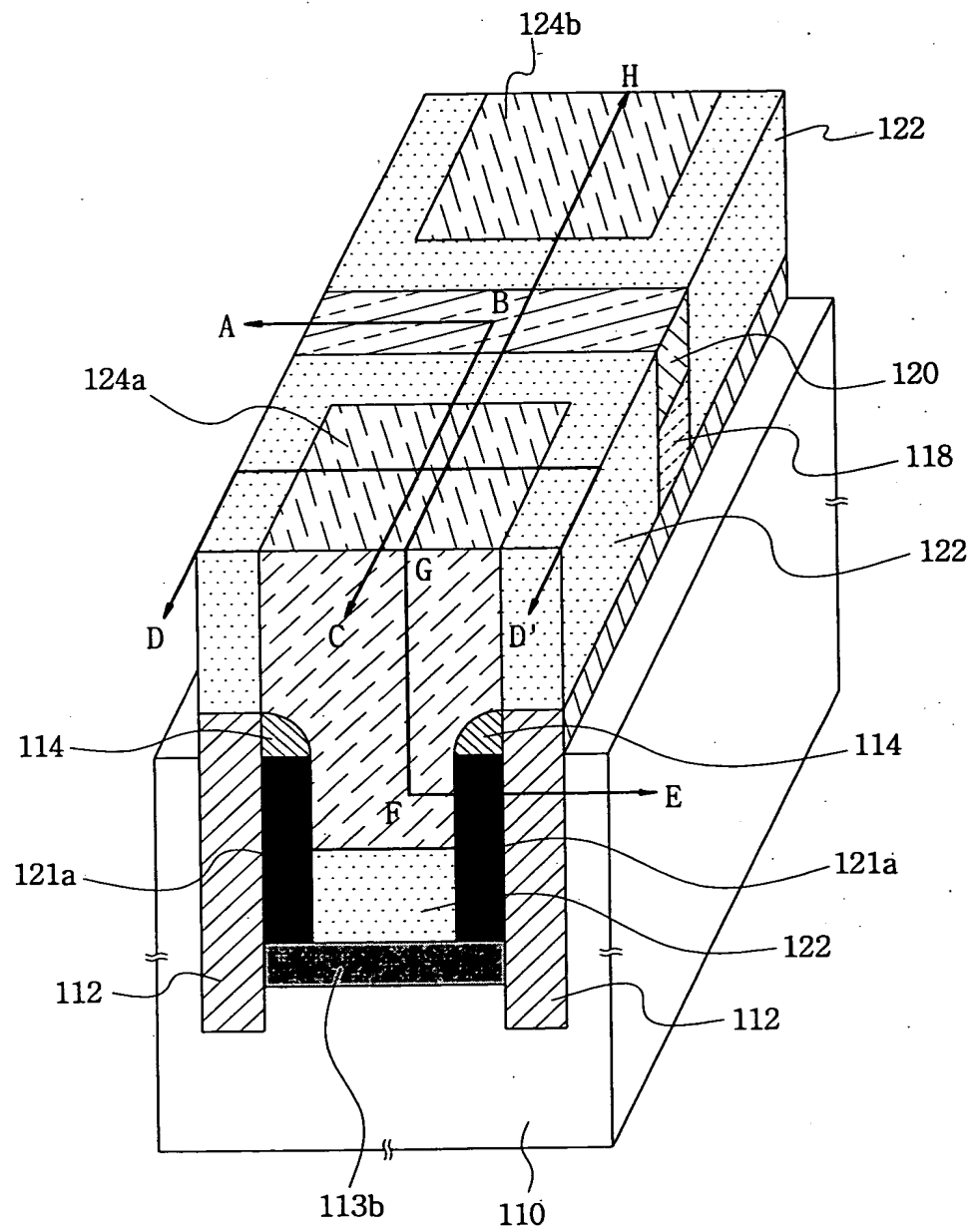


FIG. 4a

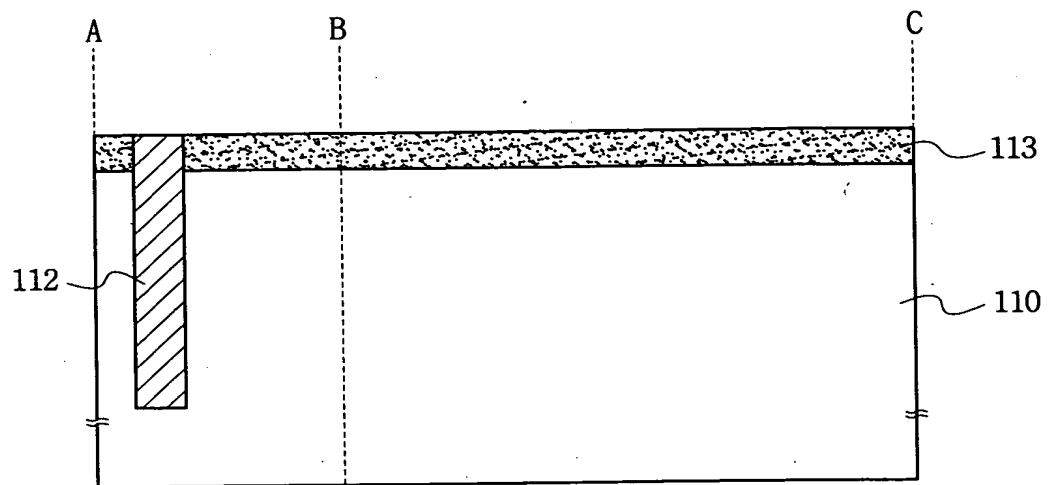


FIG. 4b

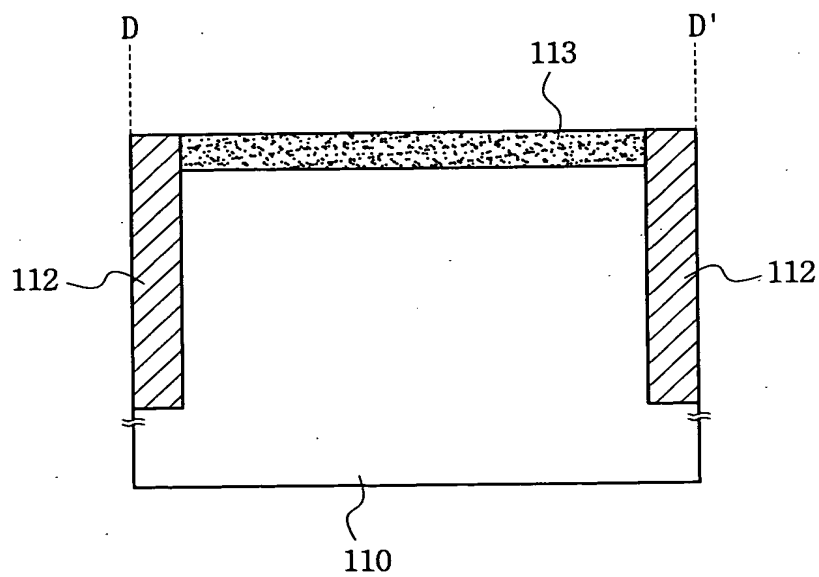


FIG. 4c

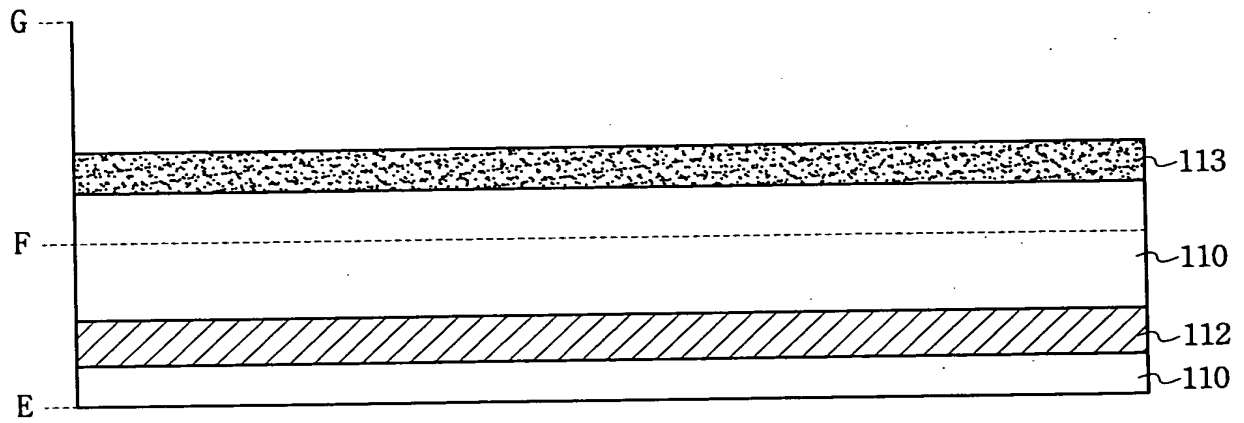


FIG. 4d

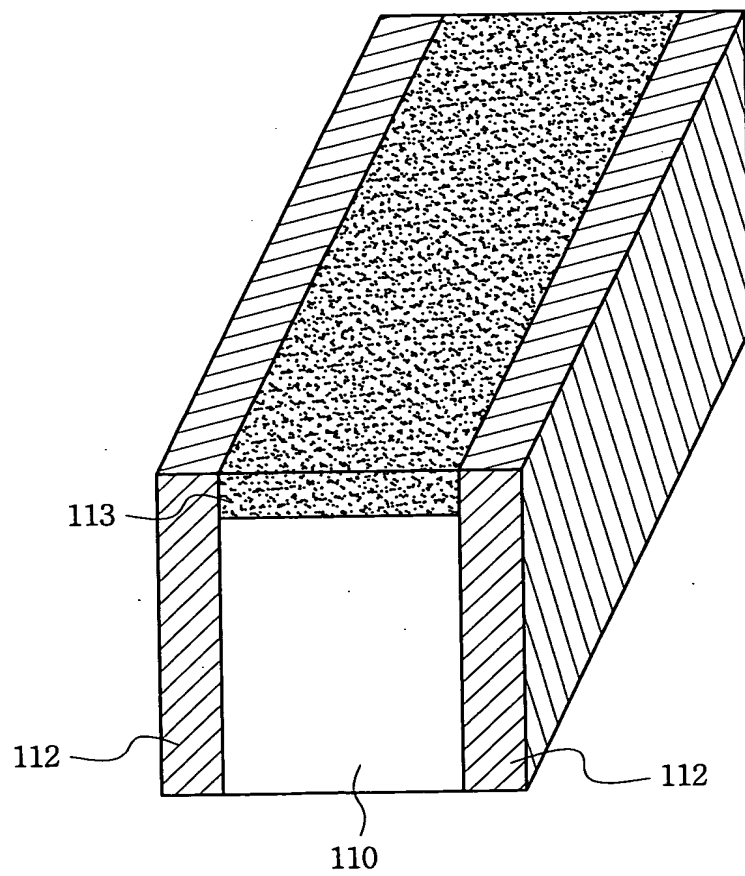


FIG. 5a

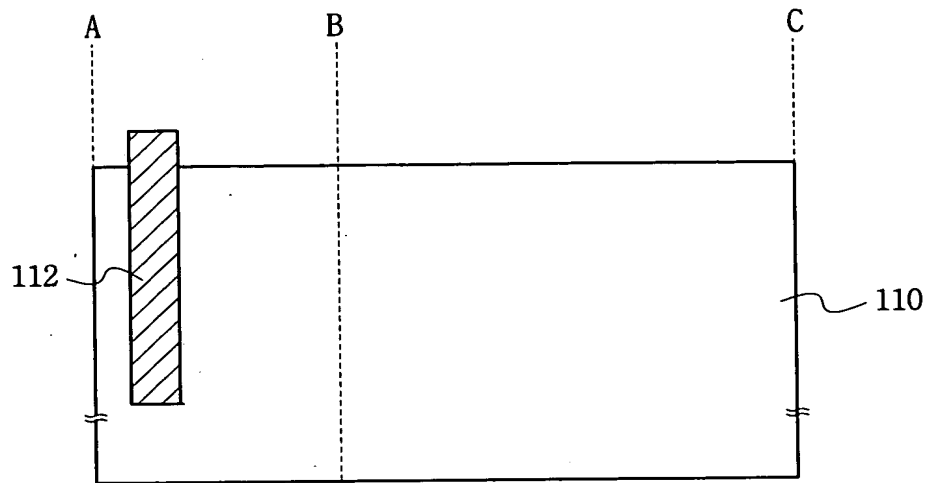


FIG. 5b

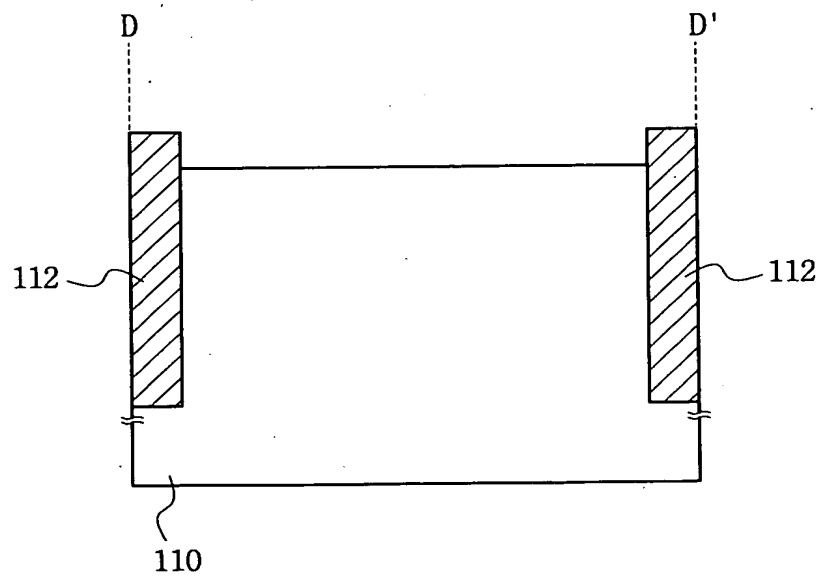


FIG. 5c

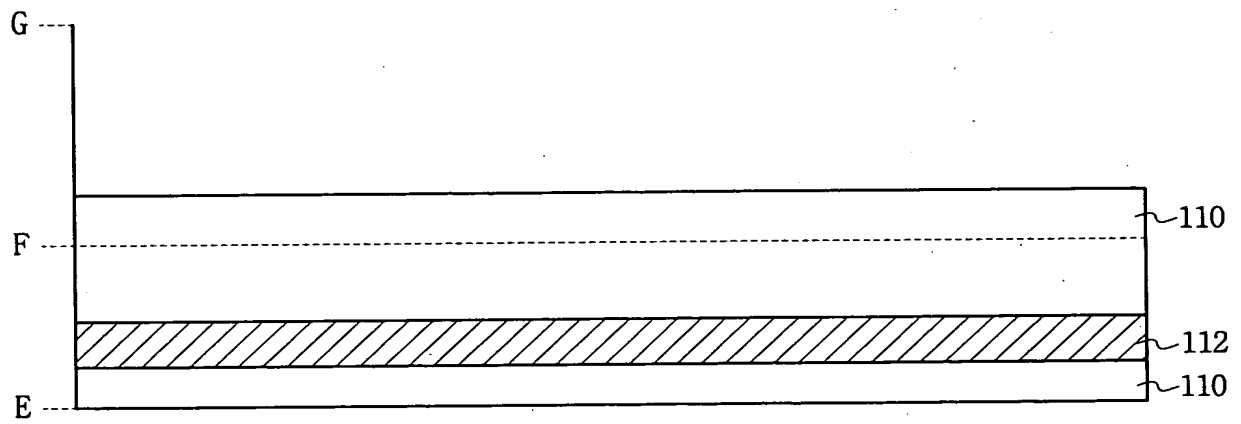


FIG. 5d

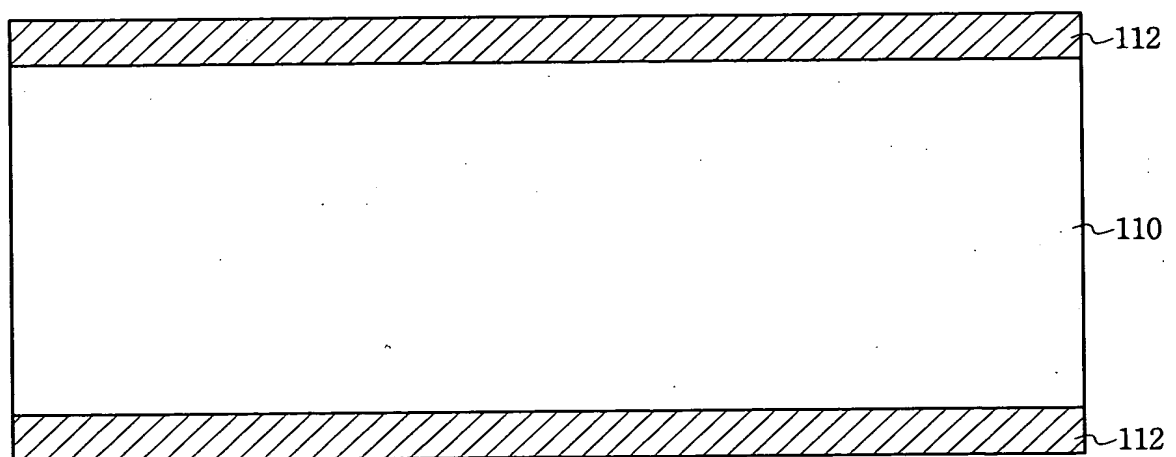


FIG. 5e

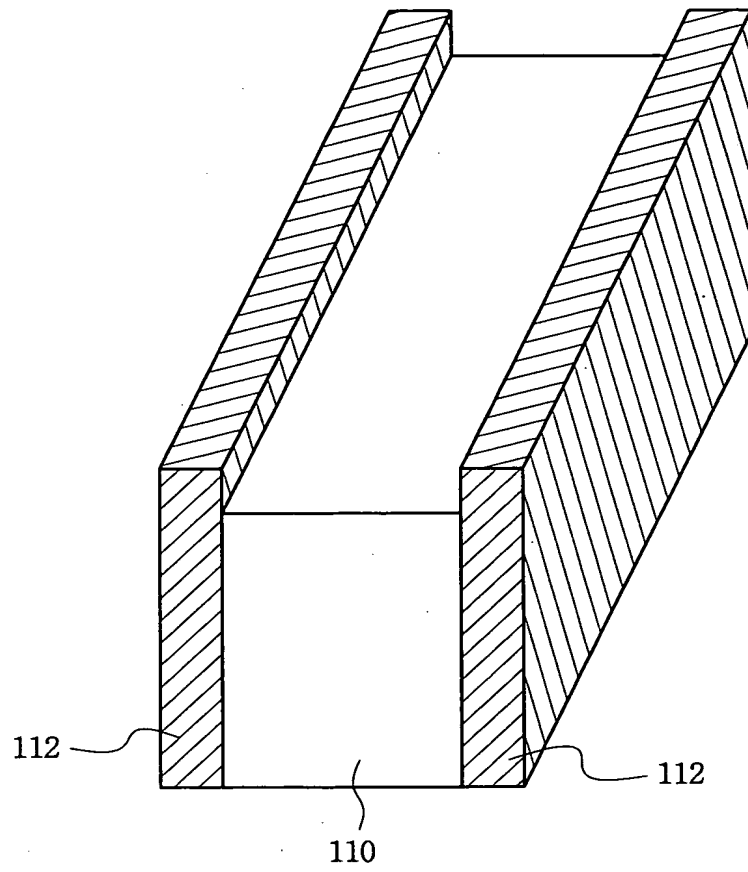


FIG. 6a

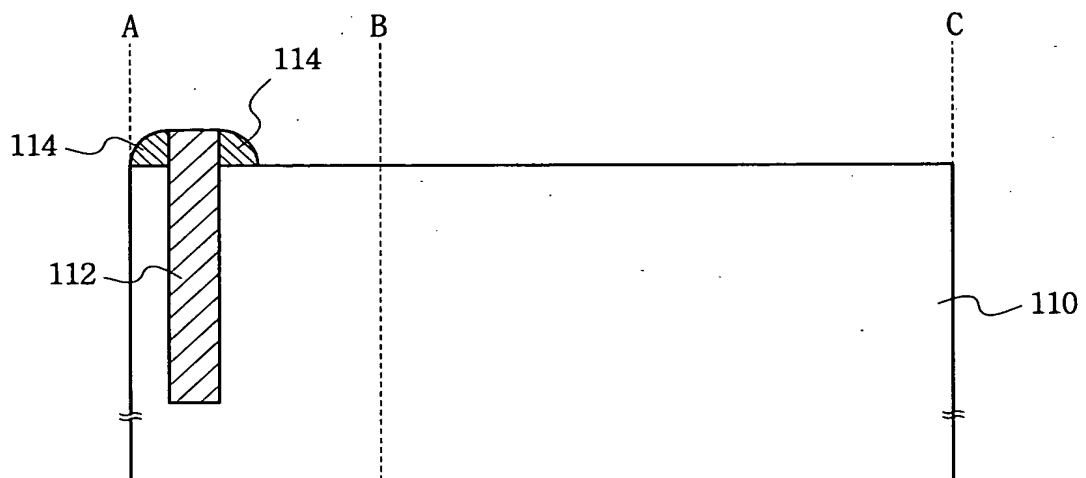


FIG. 6b

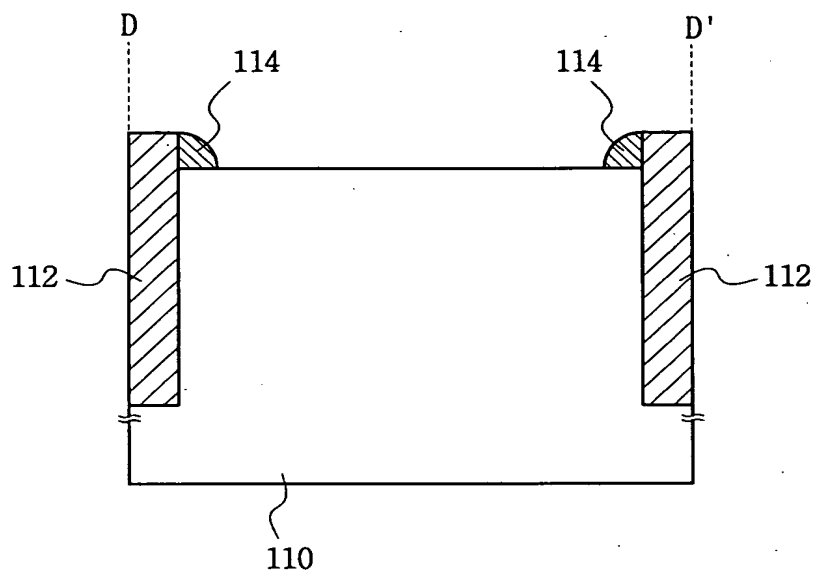


FIG. 6c

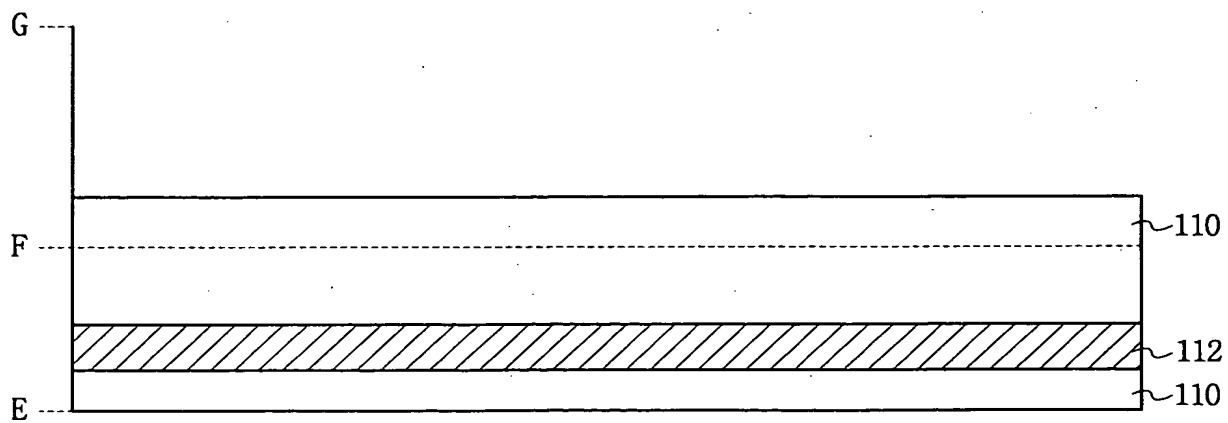




FIG. 6d

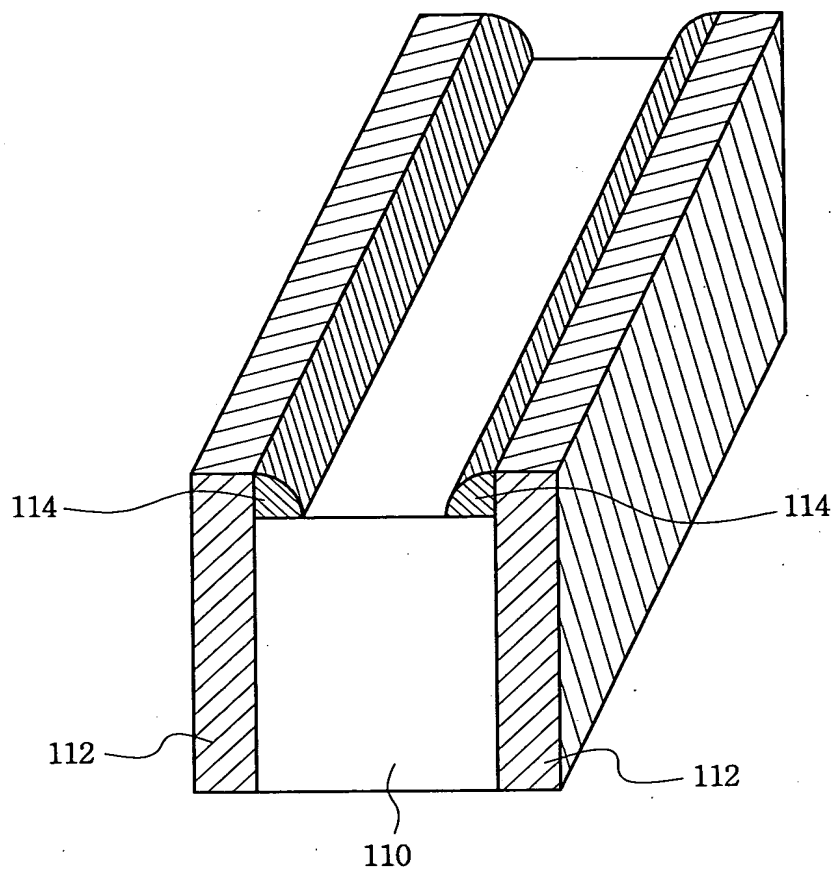


FIG. 7a

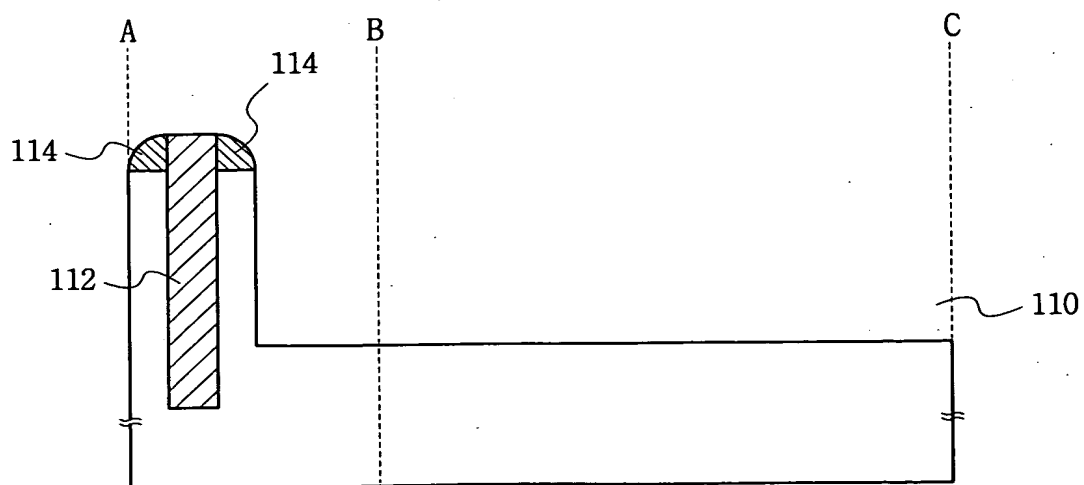


FIG. 7b

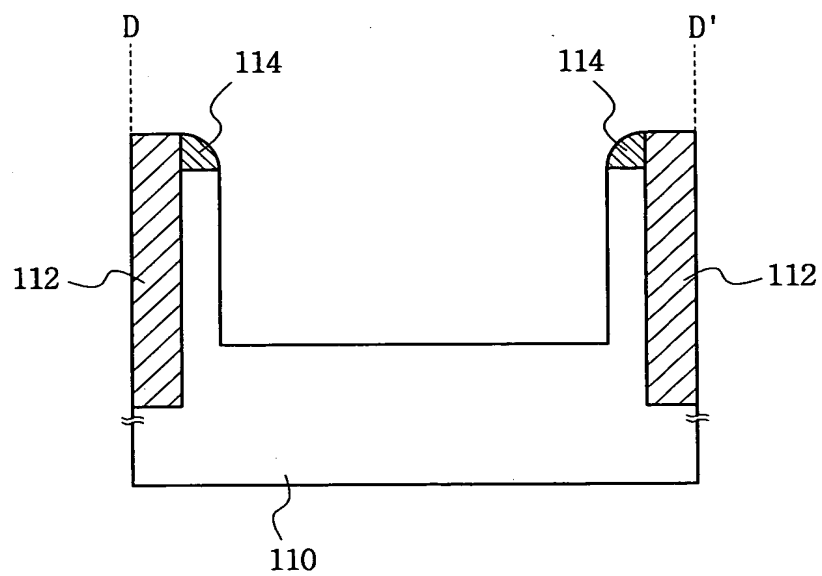


FIG. 7c

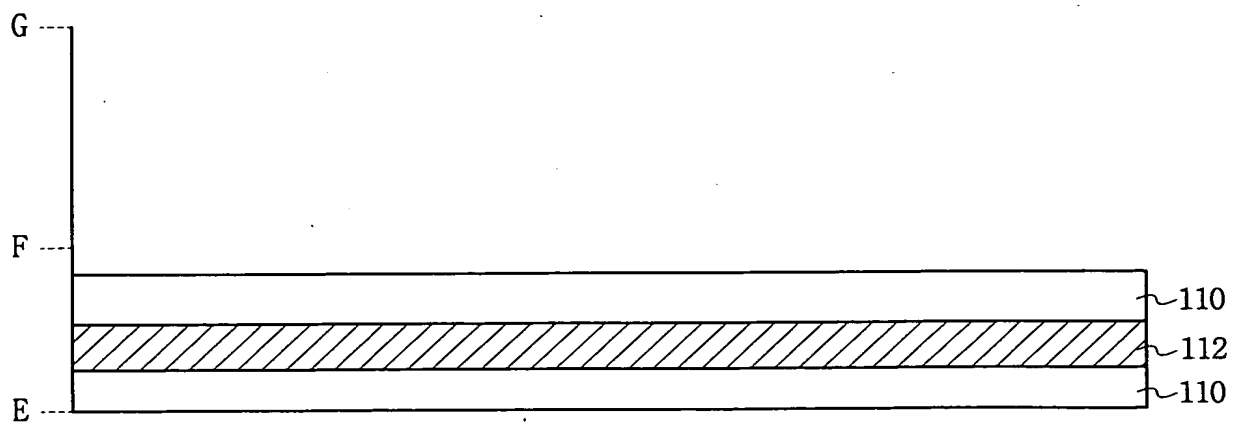


FIG. 7d

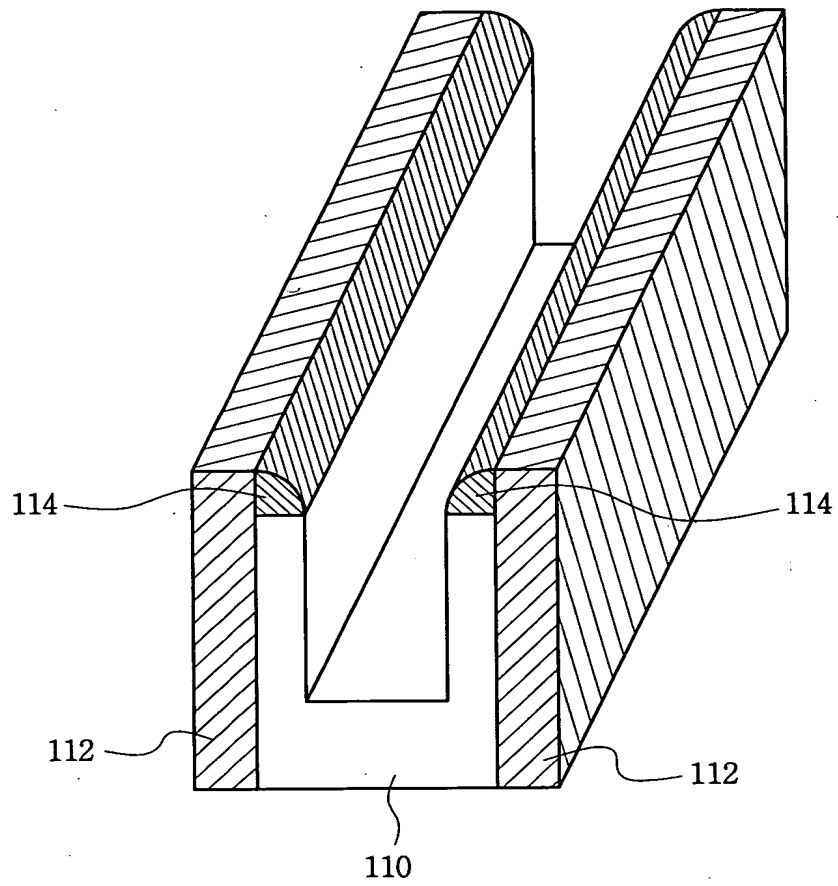


FIG. 8a

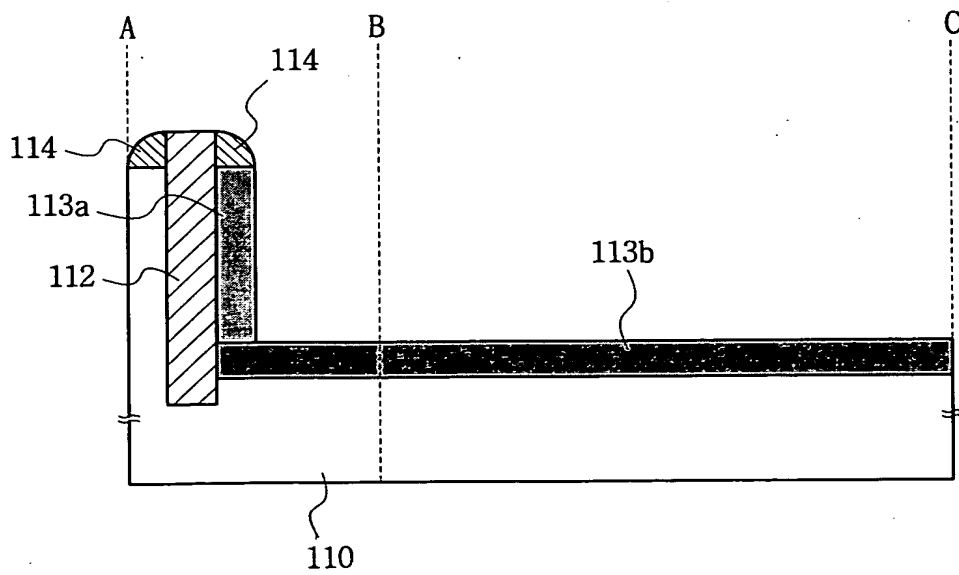


FIG. 8b

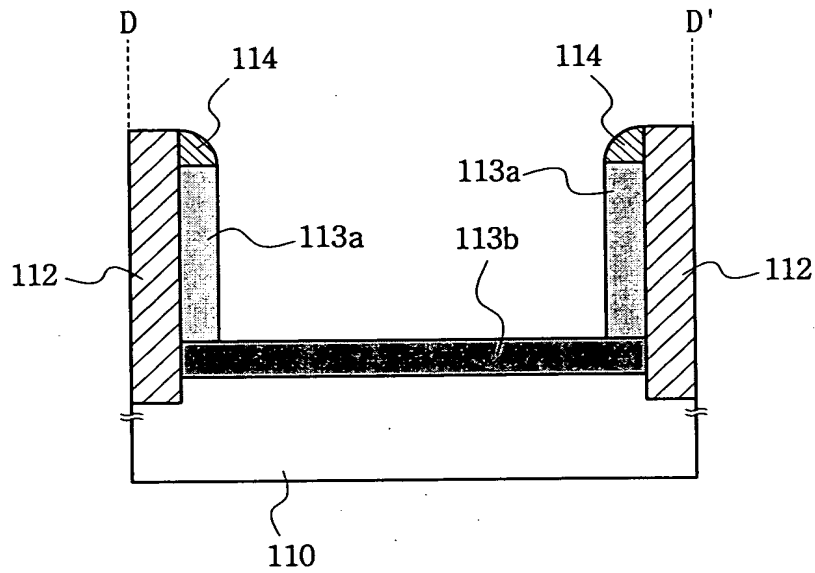


FIG. 8c

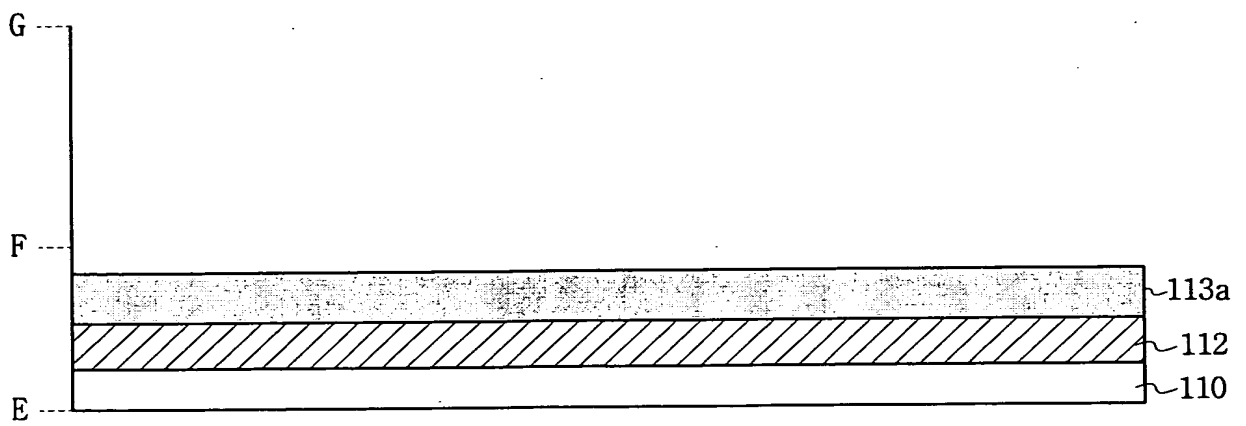


FIG. 8d

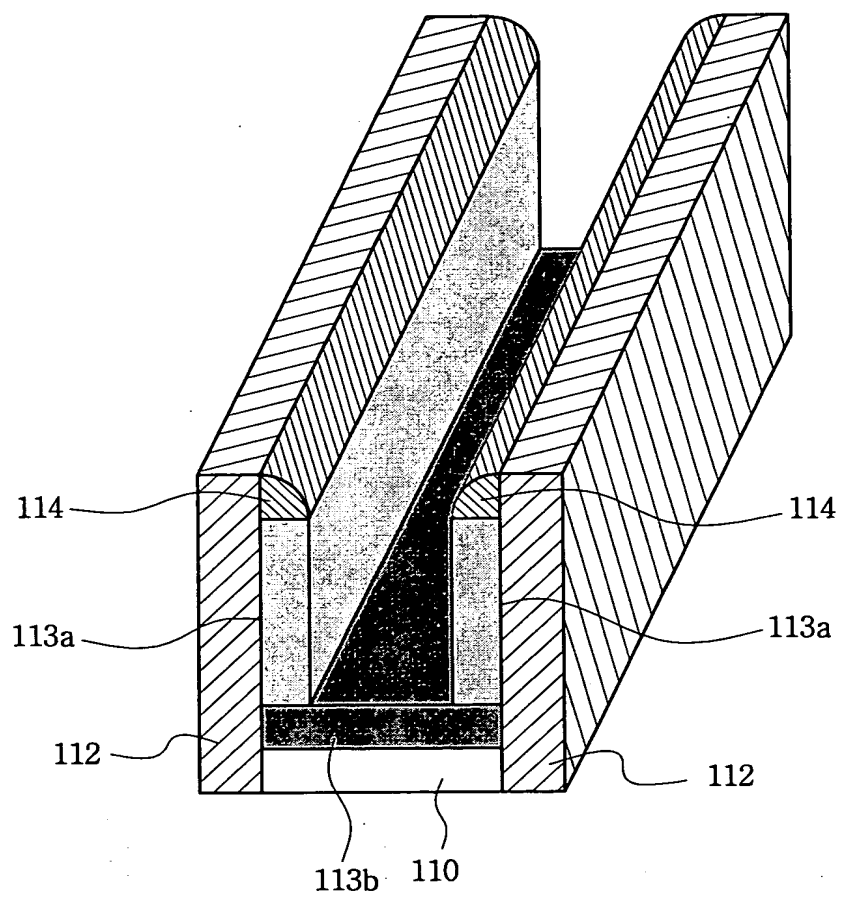


FIG. 9a

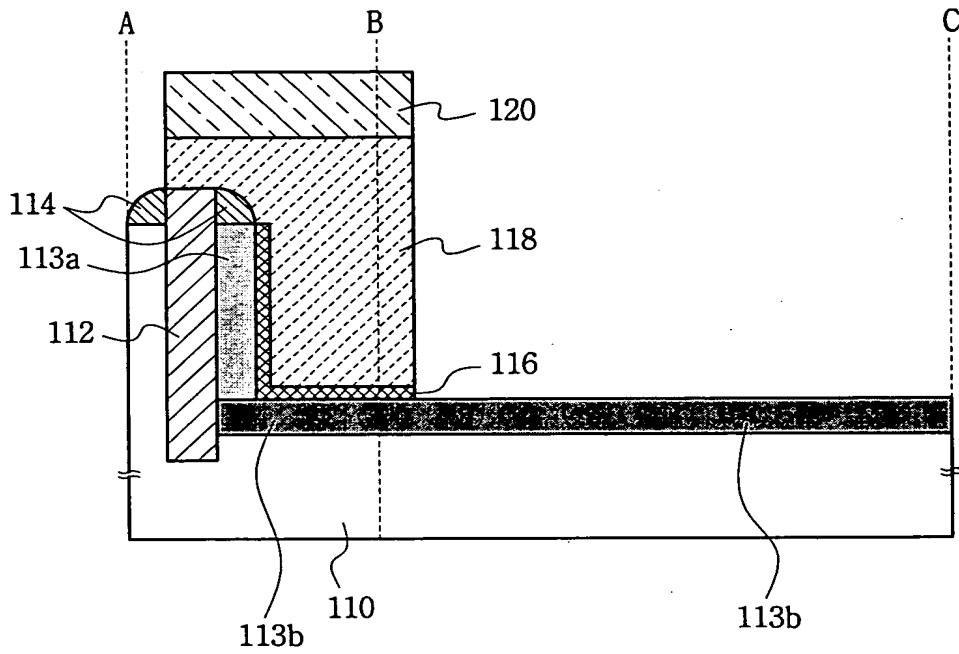


FIG. 9b

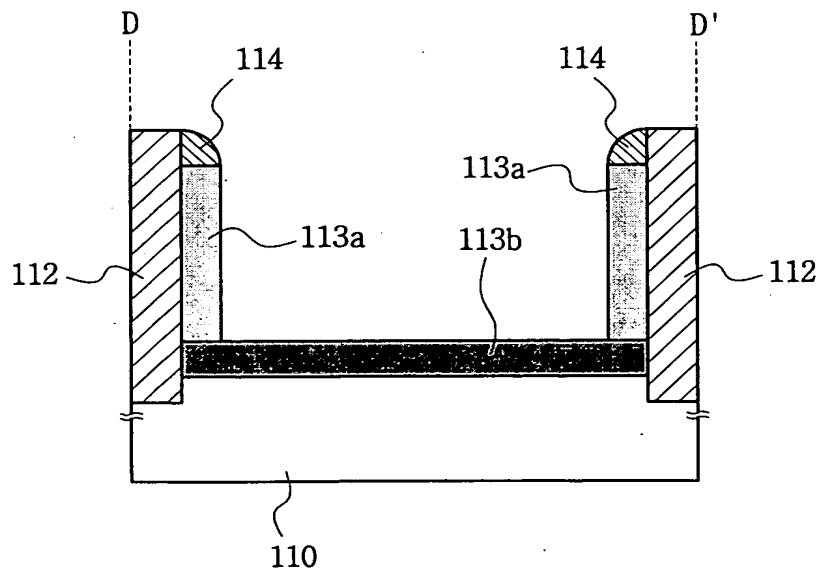


FIG. 9c

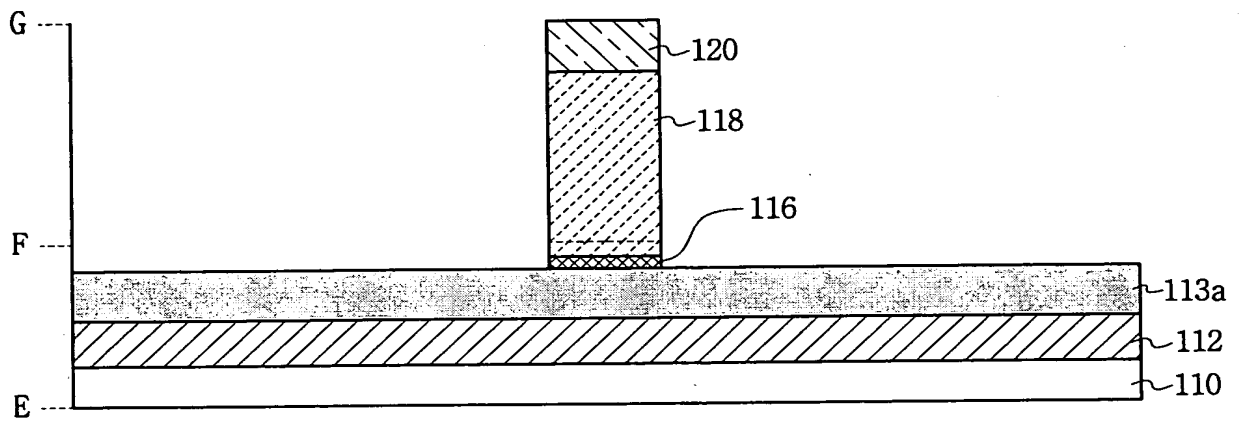


FIG. 9d

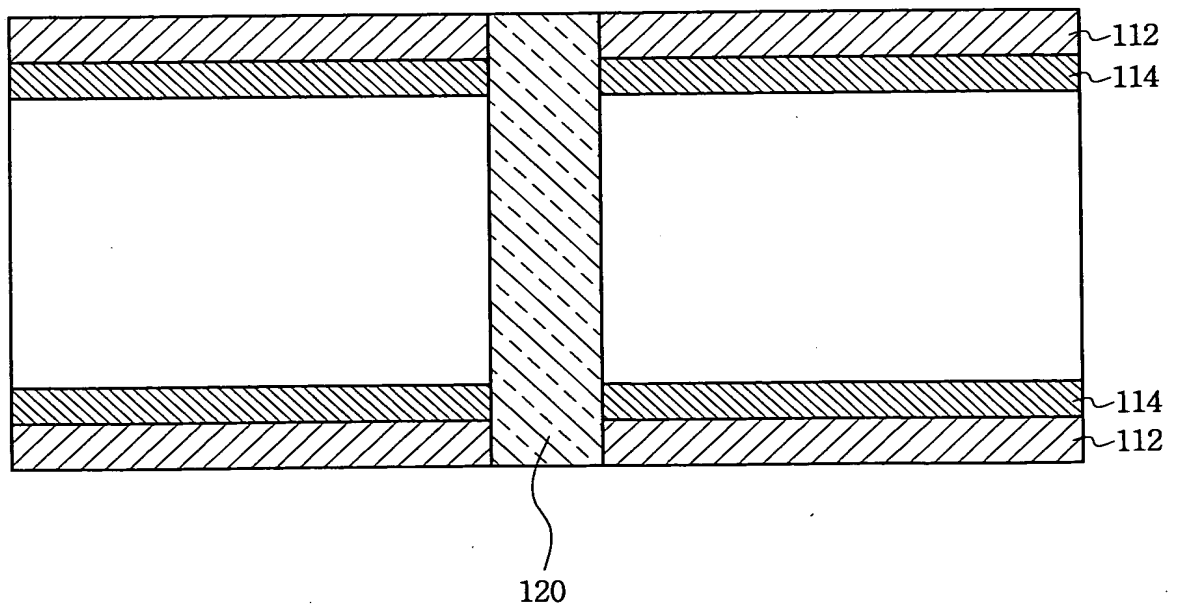
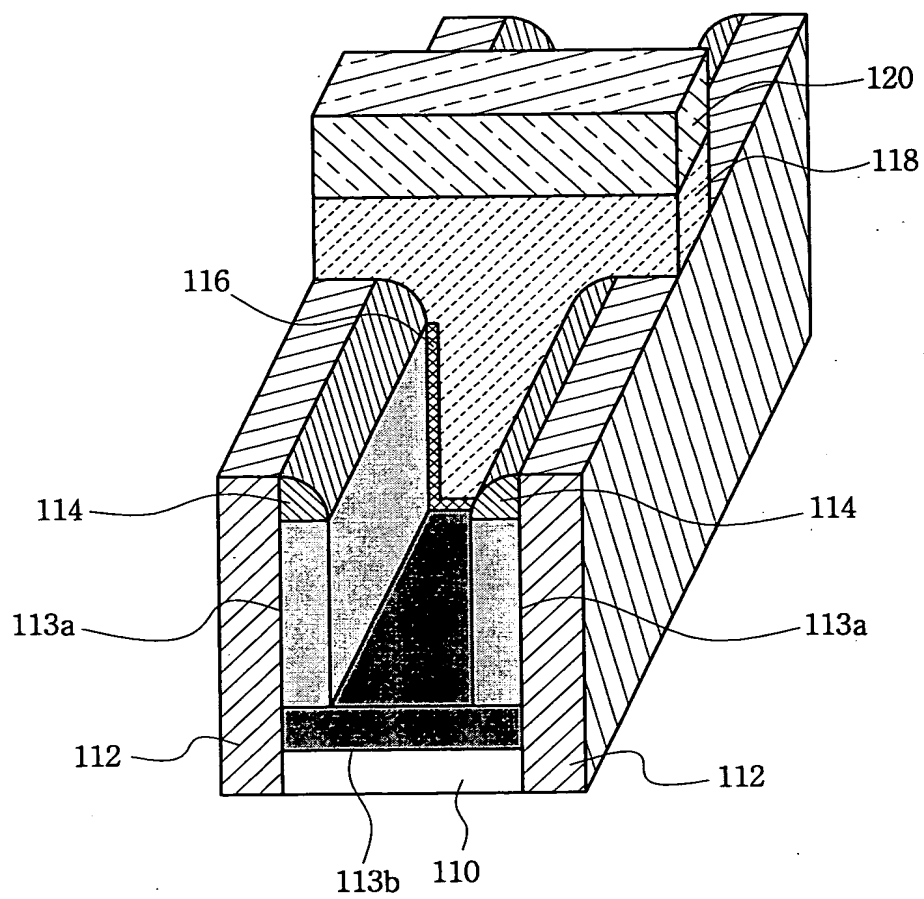


FIG. 9e





[illegible]

Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 110. A trench 113b is formed in the substrate 110. The trench 113b is lined with a conductive layer 112. The trench 113b is filled with a dielectric layer 121a. The top surface of the dielectric layer 121a is labeled 114. The trench 113b is bounded by dashed lines D and D'.

FIG. 10c

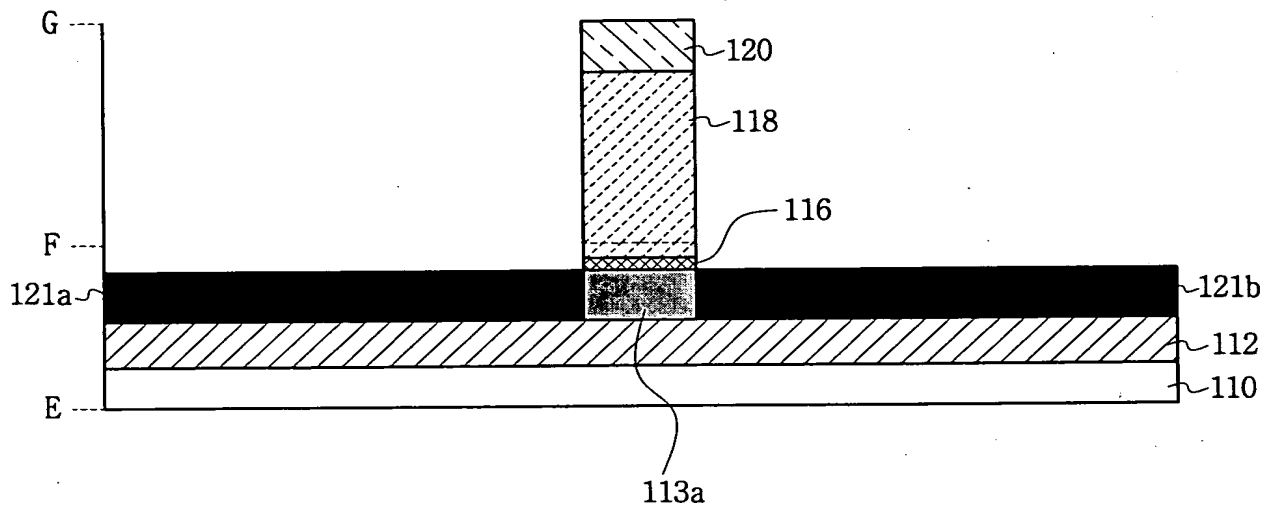


FIG. 10d

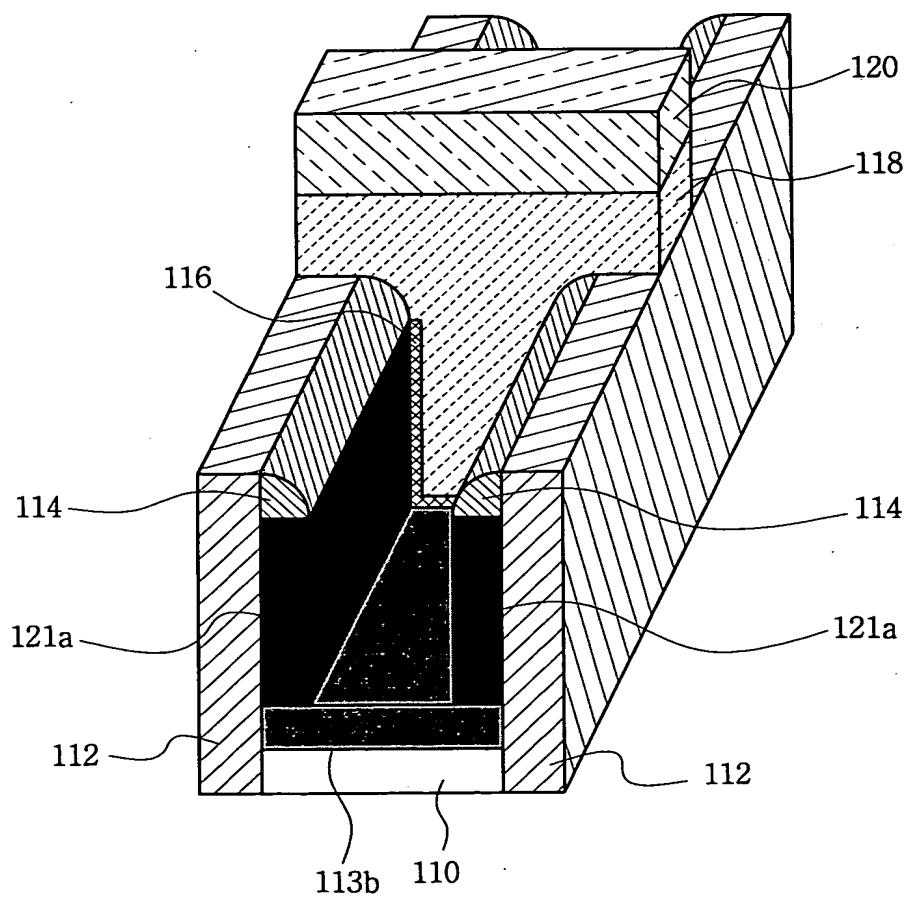


FIG. 11a

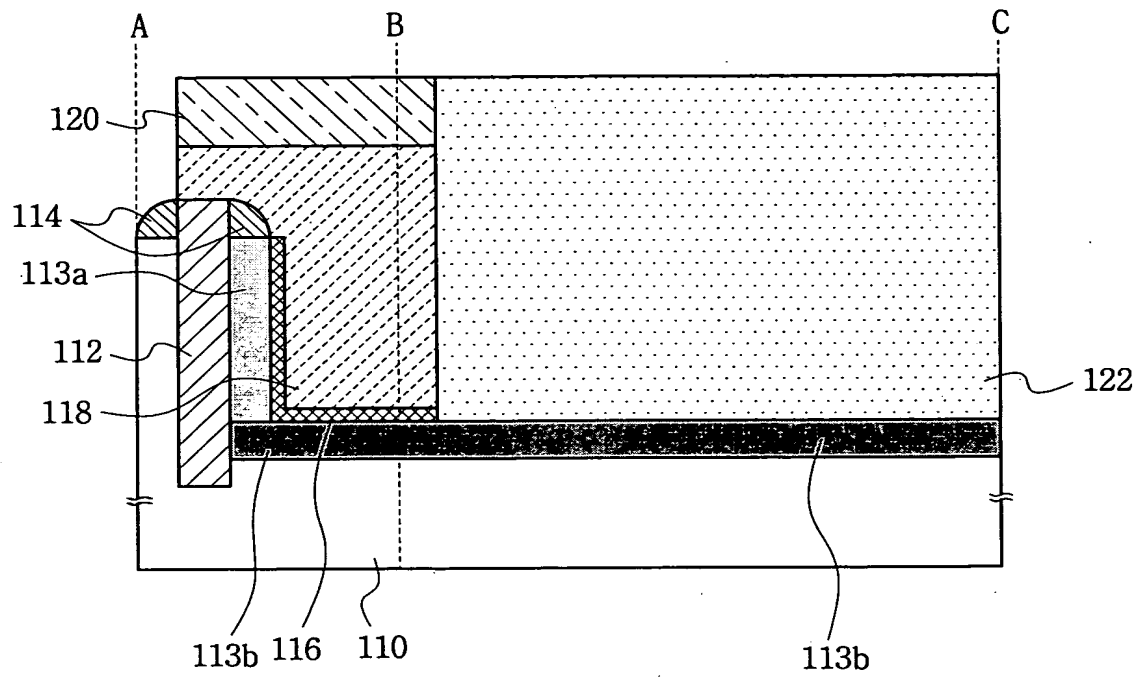


FIG. 11b

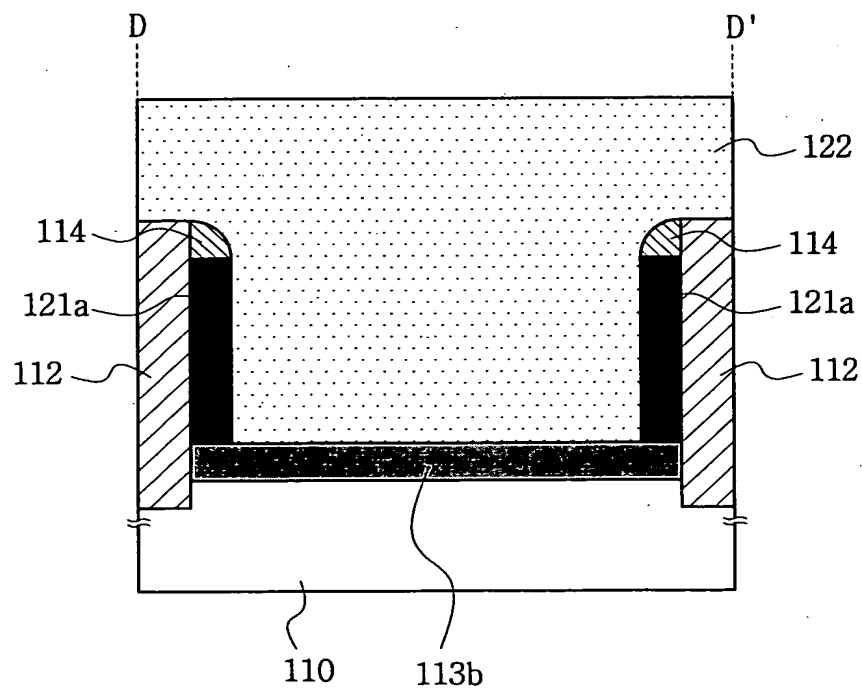


Figure 1 is a schematic diagram of a cross-section of a device. It shows a central vertical region 120 with diagonal hatching, flanked by two larger regions 122 with a stippled pattern. A label 100 is at the bottom left.

FIG. 11e

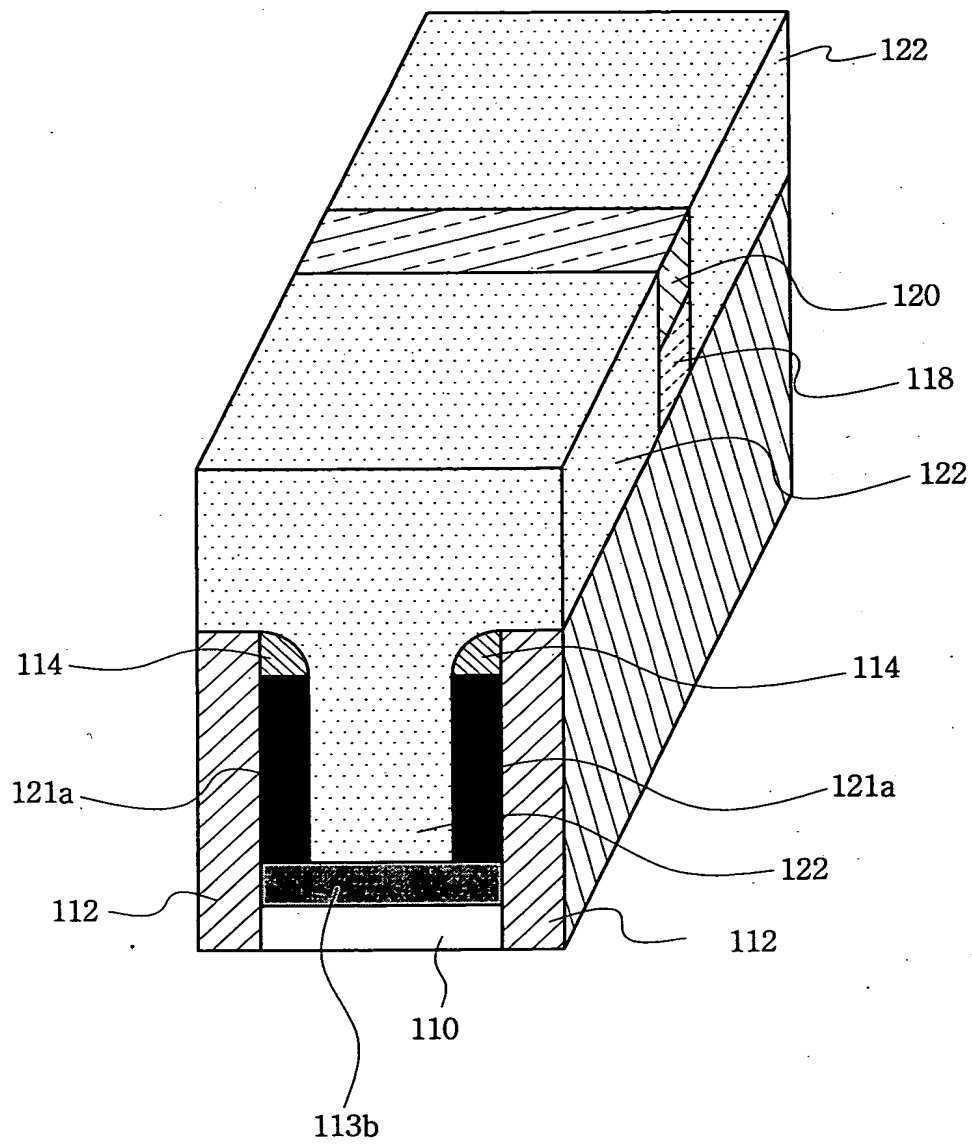


FIG. 12a

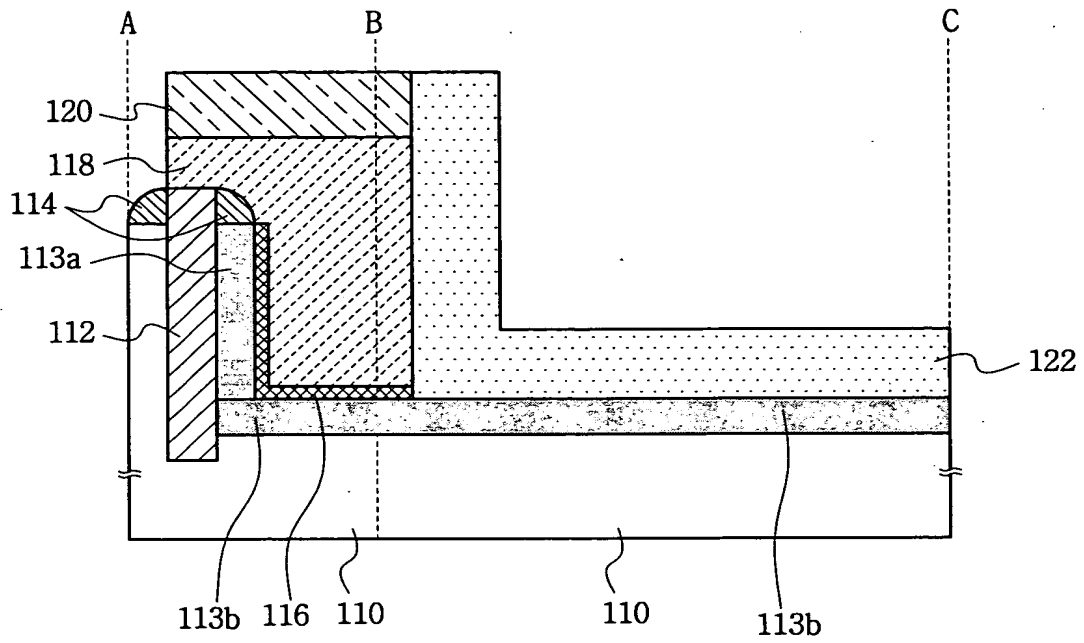


FIG. 12b

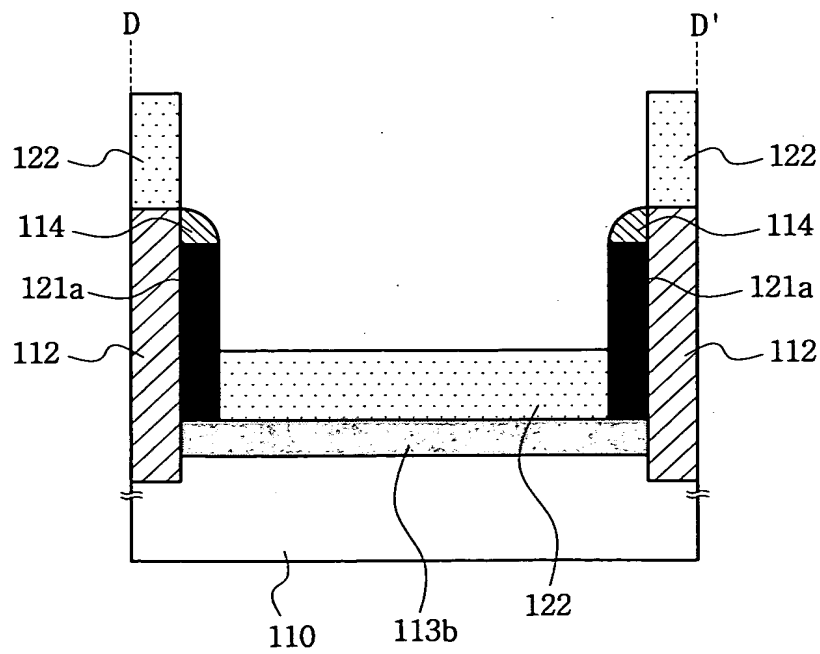


FIG. 12c

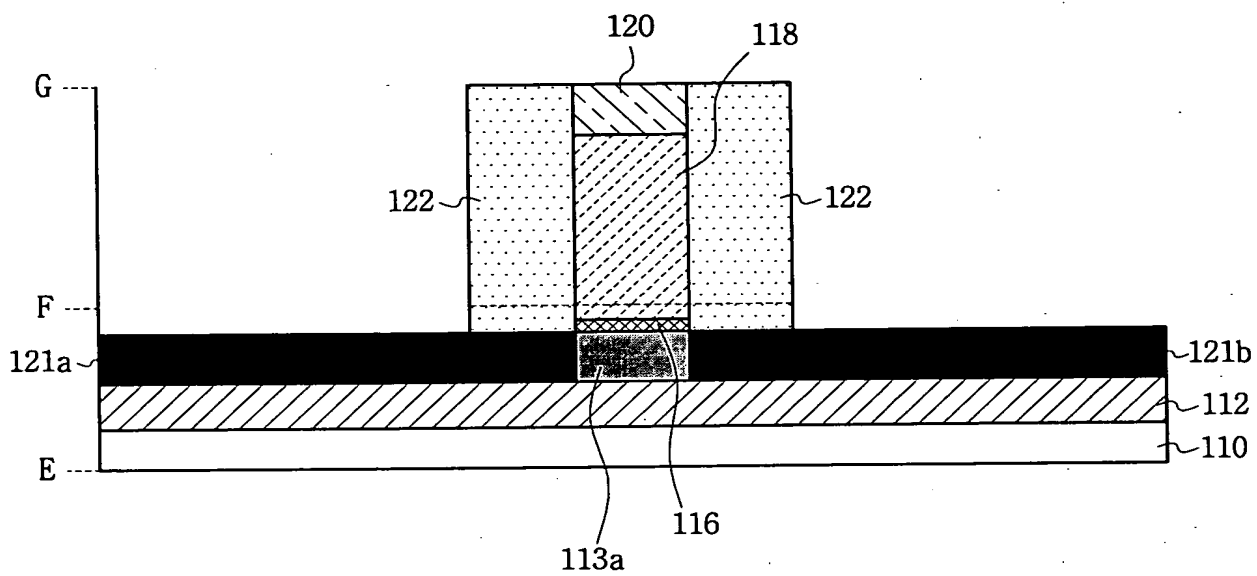


FIG. 12d

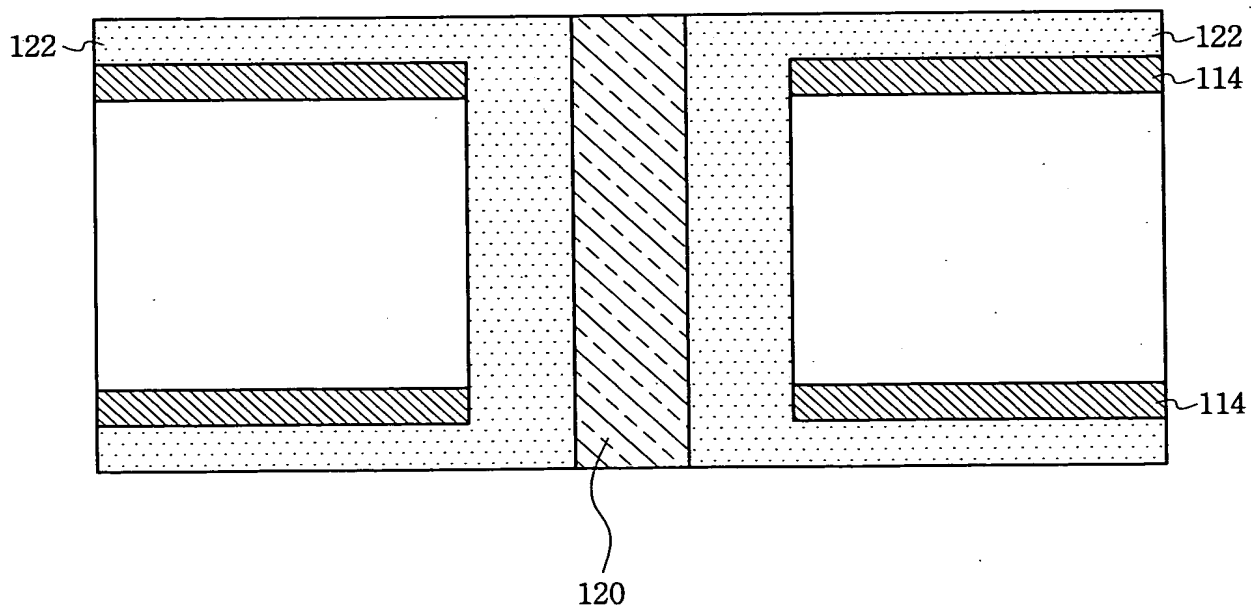
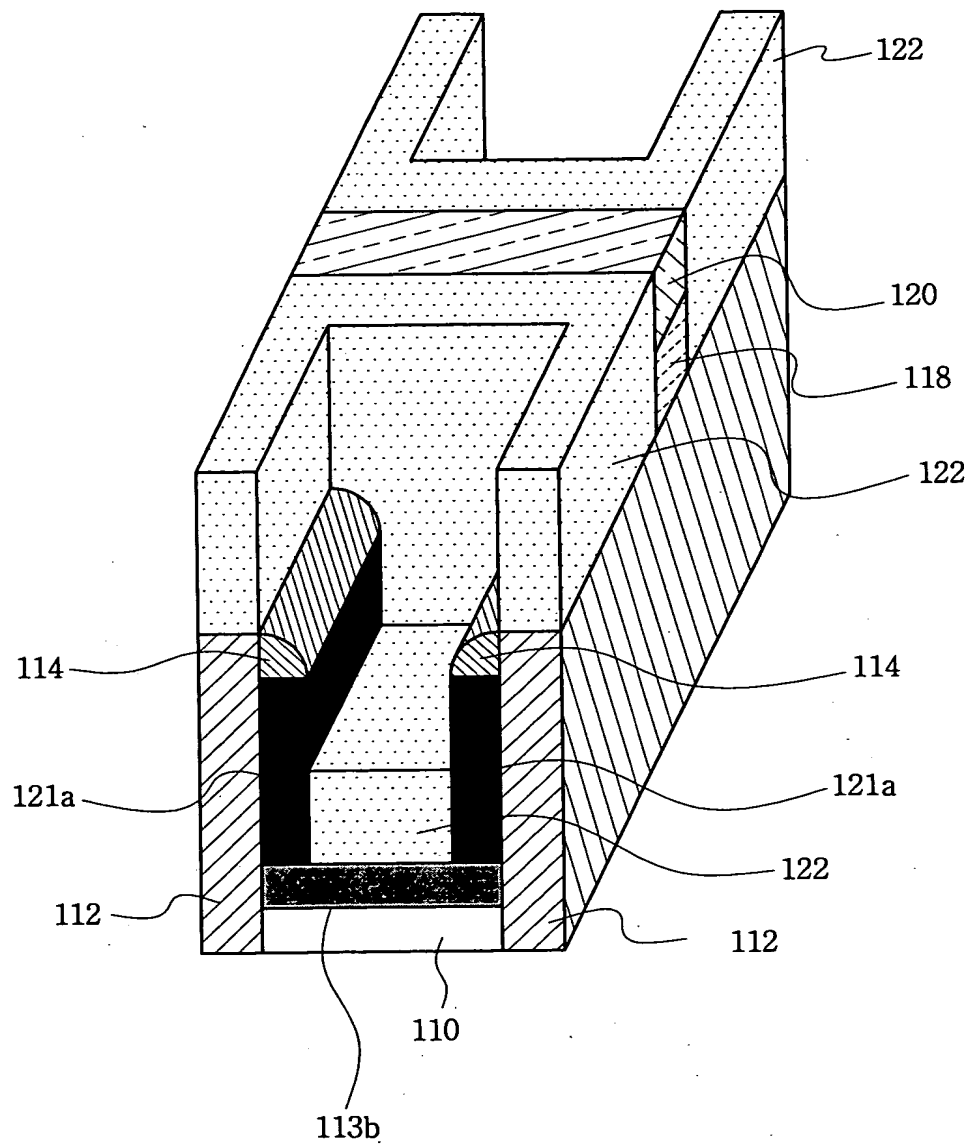


FIG. 12e





A cross-sectional view of a semiconductor device 110 taken along line D-D'. The device features a substrate 113b with a thin layer 112 on top. Two vertical pillars 121a are formed in the substrate, each with a top layer 114. The pillars are surrounded by a material 122. A layer 124a is located on top of the pillars. The device is connected to a power source 110.

FIG. 13c

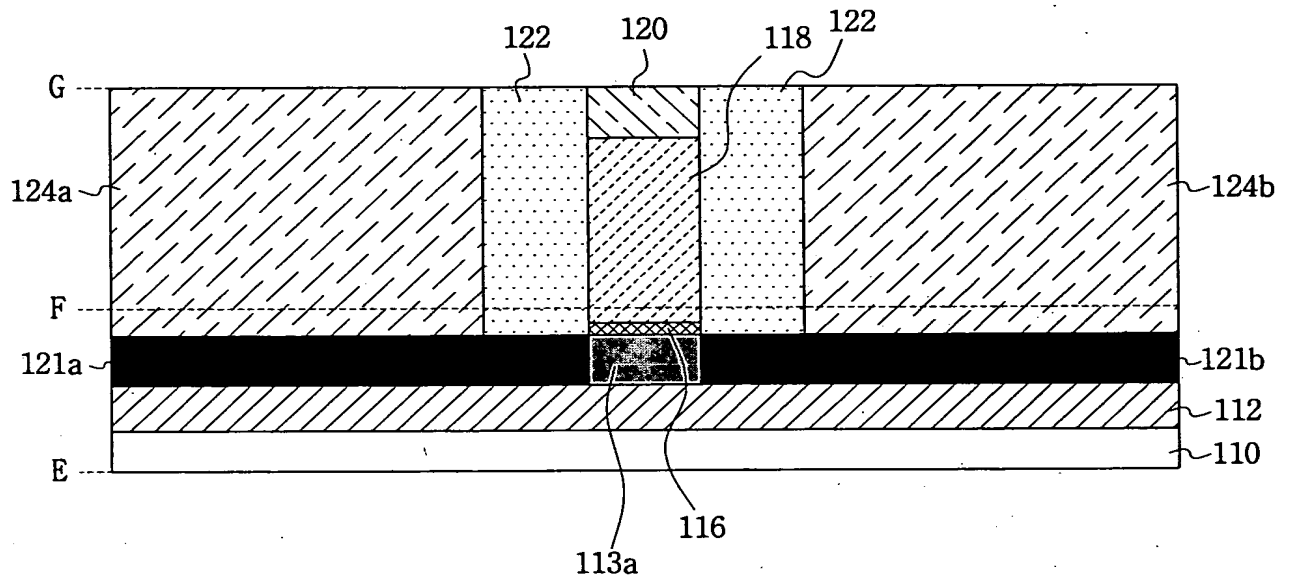


FIG. 13d

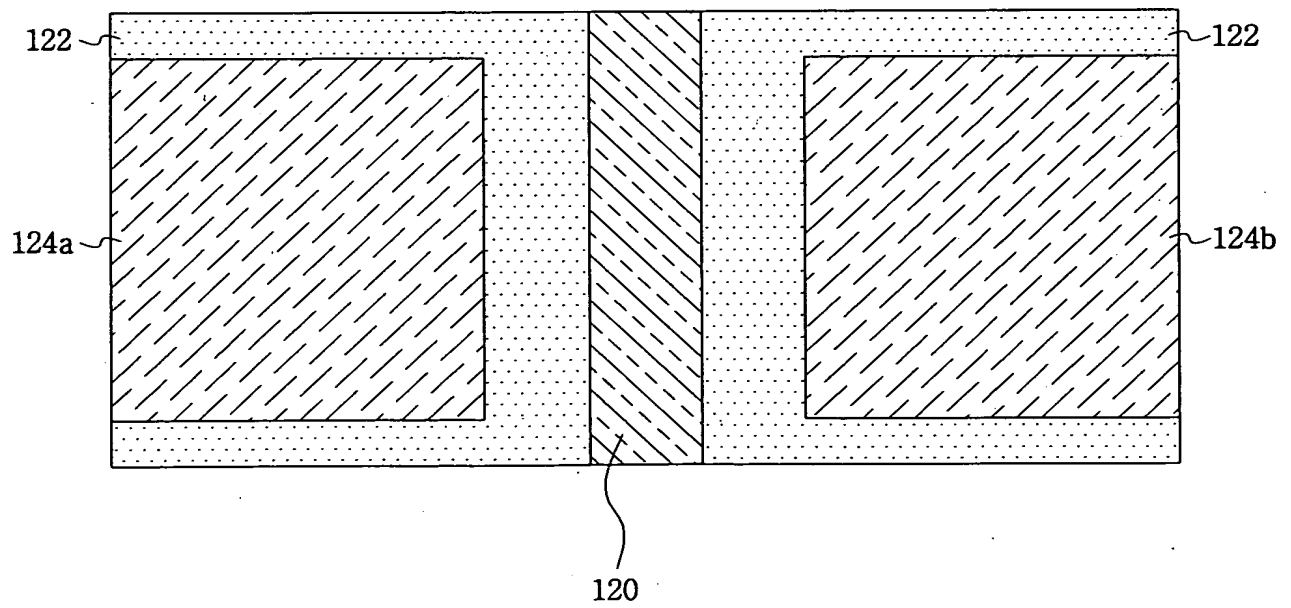


FIG. 13e

